

**METHOD AND APPARATUS FOR GENERATING TRANSACTION-BASED  
STIMULUS FOR SIMULATION OF VLSI CIRCUITS USING EVENT COVERAGE  
ANALYSIS**

**ABSTRACT OF THE DISCLOSURE**

5 The present invention applies genetic algorithmic generation of test cases the  
simulation of VLSI logic circuit blocks. The present invention generates a number of  
original test cases. This aggregate of solutions is provided to a circuit simulator. The results  
of the simulator are maintained in a matrix or table. The results detail the number of times  
that particular logic states or events associated with the VLSI block have been stimulated by  
particular test cases. The aggregate of solutions and the simulation results are then analyzed  
by the genetic algorithm. The genetic algorithm preferably identifies states associated with  
the circuit simulation that have not been produced by the original test cases. The genetic  
algorithm then combines characteristics of various test cases to generate new test cases. The  
10 new test cases are provided to the circuit simulator thereby providing a higher degree of  
confidence that the entire VLSI chip design has been simulated.